AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A data receiving system comprising:

a clock generating circuit for generating a clock whose frequency is synchronous with a frequency of a data transmission rate of a received data;

a delay circuit for delaying said received data to generate a delayed data;

a first sampling circuit for sampling said received data in response to at least one of leading and trailing edges of said clock and outputting a received data sampling value;

a second sampling circuit for sampling said delayed data in response to at least one of leading and trailing edges of said clock and outputting a delayed data sampling value; and

received data judging means for judging a received data value based on said received data sampling value and said delayed data sampling value,

wherein said received data judging means comprises:

first judging means for judging the received data value primarily based on either one of said received data sampling value and said delayed data sampling value; and

second judging means for judging the received data value secondarily based on the other of said received data sampling value and said delayed data sampling value when said first judging means fails to judge the received data value, and

said received data judging means judges the received data value with reference to same sampling values continuously appearing N times in a sampling operation.

2. (Original) The data receiving system in accordance with claim 1, wherein

said clock generating circuit is for generating a clock whose frequency is substantially identical with the frequency of the data transmission rate of said received data;

said first sampling circuit is for sampling said received data in response to both of leading and trailing edges of said clock and outputting received data sampling values; and

said second sampling circuit is for sampling said delayed data in response to both of leading and trailing edges of said clock and outputting delayed data sampling value.

3. (Original) The data receiving system in accordance with claim 1, wherein

said clock generating circuit is for generating a clock whose frequency is approximately two times the frequency of the data transmission rate of said received data;

said first sampling circuit is for sampling said received data in response to one of leading and trailing edges of said clock and outputting the received data sampling value; and

said second sampling circuit is for sampling said delayed data in response to one of leading and trailing edges of said clock and outputting delayed data sampling value.

4. (Currently Amended) A data receiving system comprising:

a clock generating circuit for generating a clock whose frequency is synchronous with a frequency of a data transmission rate of a received data;

a delay circuit for delaying said clock to generate a delayed clock;

a first sampling circuit for sampling said received data in response to at least one of leading and trailing edges of said clock and outputting a received data sampling value;

a second sampling circuit for sampling said received data in response to at least one of leading and trailing edges of said delayed clock and outputting a delayed data sampling value; and

received data judging means for judging a received data value based on said received data sampling value and said delayed data sampling value,

wherein said received data judging means comprises:

first judging means for judging the received data value primarily based on either one of said received data sampling value and said delayed data sampling value; and

second judging means for judging the received data value secondarily based on the other of said received data sampling value and said delayed data sampling value when said first judging means fails to judge the received data value, and

said received data judging means judges the received data value with reference to same sampling values continuously appearing N times in a sampling operation.

5. (Original) The data receiving system in accordance with claim 4, wherein

said clock generating circuit is for generating a clock whose frequency is substantially identical with the frequency of the data transmission rate of said received data;

said first sampling circuit is for sampling said received data in response to both of leading and trailing edges of said clock and outputting received data sampling values; and

said second sampling circuit is for sampling said received data in response to both of leading and trailing edges of said delayed clock and outputting delayed data sampling value.

6. (Original) The data receiving system in accordance with claim 4, wherein

said clock generating circuit is for generating a clock whose frequency is approximately two times the frequency of the data transmission rate of said received data;

said first sampling circuit is for sampling said received data in response to one of leading and trailing edges of said clock and outputting the received data sampling value; and

said second sampling circuit is for sampling said received data in response to one of leading and trailing edges of said delayed clock and outputting delayed data sampling value.

7. (New) The data receiving system in accordance with claim 1, wherein said N is an even number, and it is judged that said same sampling value is continuously received (N/2) times.

8. (New) The data receiving system in accordance with claim 1, wherein said N is an odd number, and it is judged that said sampling value is continuously received ((N-1)/2) times or ((N+1)/2) times.

9. (New) The data receiving system in accordance with claim 4, wherein said N is an even number, and it is judged that said same sampling value is continuously received (N/2) times.

10. (New) The data receiving system in accordance with claim 4, wherein said N is an odd number, and it is judged that said sampling value is continuously received ((N-1)/2) times or ((N+1)/2) times.